IN THE CLAIMS:

Please amend the claims as follows: (All claims listed)

1. (Currently Amended) A hardware processor comprising:

a plurality of programmable logic arrays (PLAs);

an instruction pointer queue coupled to said plurality of PLAs;

an instruction pointer sequencing logic/predictor component coupled to said instruction pointer queue;

a micro-operation cache coupled to said instruction pointer sequencing logic/predictor component;

a micro-operation memory coupled to said micro-operation cache, said micro-operation cache to store a subset of micro-operations to be stored in said micro-operation memory; and

a trace pipe (TPIPE) coupled to said micro-operation cache and said instruction pointer queue, said trace pipe to assemble micro-operations for an instruction into an instruction trace to be forwarded for execution.

2. (Currently Amended) A hardware processor comprising:

a plurality of programmable logic arrays (PLAs) wherein said plurality of PLAs are coupled to a plurality of streaming buffers and said plurality of PLAs are to provide an instruction pointer for a first micro-operation in each instruction and predict a number of micro-operations between the first micro-operation and a last micro-operation in each instruction;

an instruction pointer queue coupled to said plurality of PLAs;

an instruction pointer sequencing logic/predictor component coupled to said instruction pointer queue;

a micro-operation cache coupled to said instruction pointer sequencing logic/predictor component;

a micro-operation memory coupled to said micro-operation cache; and

a trace pipe (TPIPE) coupled to said micro-operation cache and said instruction pointer queue.

3. (Original) The processor of claim 1 wherein said plurality of PLAs are coupled to an alias logic component.

4. (Original) The processor of claim 1 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

5. (Original) The processor of claim 3 wherein said instruction pointer queue is at least three micro-instruction pointers wide.

6. (Original) The processor of claim 1 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor coupled to said four-to-one multiplexer, said micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component coupled to said four-to-one multiplexer, said incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

7. (Previously Presented) The processor of claim 6 wherein said four-to-one multiplexer is further to receive a next micro-instruction pointer from said micro-operation memory.

8. (Original) The processor of claim 1 wherein said micro-operation cache comprises:

an at least 3-wide micro-operation cache to store commonly used micro-operations.

9. (Original) The processor of claim 1 wherein said micro-operation memory comprises:

an at least 3-wide micro-operation read only memory to store all micro-operations that can be decoded from an instruction set.

10. (Original) The processor of claim 1 further comprising:

a patch cache coupled to said micro-operation cache.

11. (Currently Amended) A hardware processor comprising:

a plurality of programmable logic arrays (PLAs) to output a first instruction pointer for a first micro-instruction operation in each instruction;

an instruction pointer queue to receive the first instruction pointers;

an instruction pointer sequencing logic/predictor component to predict a next instruction pointer for each instruction;

a micro-operation cache to store a plurality of frequently used micro-instruction operations;

a micro-operation memory to store a plurality of micro-instruction operations, said micro-operation cache to store a subset of micro-operations to be stored in said micro-operation memory; and

a trace pipe (TPIPE) to [[.]]assemble micro-operations for an instruction into an instruction trace to be forwarded for execution.

12. (Original) The processor of claim 11 wherein each of said plurality of PLAs to receive input from a build pipe.

13. (Original) The processor of claim 11 wherein each of said plurality of PLAs receive input from an alias logic component.

14. (Original) The processor of claim 11 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

15. (Original) The processor of claim 14 wherein said instruction pointer queue is to concurrently provide up to three micro-instruction pointers.

16. (Original) The processor of claim 11 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

17. (Previously Presented) The processor of claim 16 wherein said four-to-one multiplexer is further to receive a next micro-instruction pointer from said micro-operation memory.

18. (Original) The processor of claim 11 wherein said micro-operation cache is to store at least 3 micro-operations per set of commonly used micro-operations.

19. (Original) The processor of claim 11 wherein said micro-operation read only memory is store at least 3 micro-operations per set of all micro-operations that can be decoded from an instruction set.

20. (Previously Presented) The processor of claim 11 further comprising:

a patch cache to store micro-operations and to be read in parallel with said micro-operation memory.

21. (Previously Presented) A method comprising:

storing in a cache a plurality of commonly used micro-operations;

storing a plurality of micro-operations in a separate micro-operation memory, said cache storing a subset of the micro-operations stored in said separate micro-operation memory;

determining a first instruction pointer for a first operation in an instruction;

storing the first instruction pointer;

predicting a next instruction pointer for each additional operation in the instruction;

reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers; and

assembling trace with a trace pipe (TPIPE) micro-operations for an instruction into an instruction to be forwarded for execution.

22. (Cancelled)

23. (Original) The method of claim 21 wherein determining a first instruction pointer for a first operation in an instruction comprises:

determining the first instruction pointer for the first operation in the instruction in a programmable logic array.

24. (Previously Presented) The method of claim 21 wherein predicting a next instruction pointer for each additional operation in the instruction comprises:

predicting the next instruction pointer for each additional operation in the instruction in a predictor separate from the programmable logic array.

25. (Original) The method of claim 24 wherein reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers comprises:

reading the one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers from a cache memory or a read only memory, if the one or more operations are not in the cache memory.

26. (Previously Presented) A machine-readable memory having stored thereon a plurality of executable instructions to perform a method comprising:

storing in a cache a plurality of commonly used micro-operations;

storing a plurality of micro-operations in a separate micro-operation memory, said cache storing a subset of the micro-operations stored in said separate micro-operation memory;

determining a first instruction pointer for a first operation in an instruction;

storing the first instruction pointer;

predicting a next instruction pointer for each additional operation in the instruction;

reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers; and

assembling trace with a trace pipe (TPIPE) micro-operations for an instruction into an instruction to be forwarded for execution.

27. (Cancelled) .

28. (Currently Amended) The machine-readable ~~medium~~ memory of claim 26 wherein determining a first instruction pointer for a first operation in an instruction comprises:

determining the first instruction pointer for the first operation in the instruction in a programmable logic array.

29. (Currently Amended) The machine-readable ~~medium~~ memory of claim 26 wherein predicting a next instruction pointer for each additional operation in the instruction comprises:

predicting the next instruction pointer for each additional operation in the instruction in a predictor separate from the programmable logic array.

30. (Currently Amended) The machine-readable ~~medium~~ memory of claim 29 wherein reading one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers comprises:

reading the one or more operations in the instruction using the first instruction pointer and any predicted next instruction pointers from a cache memory or a read only memory, if the one or more operations are not in the cache memory.

31. (Currently Amended) A computer system comprising:

a memory to provide program instructions; and

a hardware processor coupled to said memory, said processor comprising:

a plurality of programmable logic arrays (PLAs);

an instruction pointer queue coupled to said plurality of PLAs;

an instruction pointer sequencing logic/predictor component coupled to said instruction pointer queue;

a micro-operation cache coupled to said instruction pointer sequencing logic/predictor component;

a micro-operation memory coupled to said micro-operation cache, said micro-operation cache to store a subset of micro-operations to be stored in said micro-operation memory; and

a trace pipe (TPIPE) coupled to said micro-operation cache and said instruction pointer queue, said trace pipe to assemble micro-operations for an instruction into an instruction trace to be forwarded for execution.

32. (Currently Amended) A computer system comprising:

a memory to provide program instructions; and

a hardware processor coupled to said memory, said processor comprising:

a plurality of programmable logic arrays (PLAs), wherein said plurality of PLAs are coupled to a plurality of streaming buffers and said plurality of PLAs are to provide an instruction pointer for a first micro-operation in each program instruction and predict a number of micro-operations between the first micro-operation and a last micro-operation in each instruction;

an instruction pointer queue coupled to said plurality of PLAs;

an instruction pointer sequencing logic/predictor component coupled to said instruction pointer queue;

a micro-operation cache coupled to said instruction pointer sequencing logic/predictor component;

a micro-operation memory coupled to said micro-operation cache; and

a trace pipe (TPIPE) coupled to said micro-operation cache and said instruction pointer queue.

33. (Currently Amended) The ~~processor~~ computer system of claim 31 wherein said plurality of PLAs are coupled to an alias logic component.

34. (Currently Amended) The ~~processor~~ computer system of claim 31 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

35. (Currently Amended) The ~~processor~~ computer system of claim 31 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor coupled to said four-to-one multiplexer, said micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component coupled to said four-to-one multiplexer, said incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

36. (Currently Amended) The ~~processor~~ computer system of claim 31 further comprising:

a patch cache coupled to said micro-operation cache.

37. (Currently Amended) A computer system comprising:

a memory to provide program instructions; and

a hardware processor coupled to said memory, said processor comprising:

a plurality of programmable logic arrays (PLAs) to output a first instruction pointer for a first micro-instruction operation in each instruction;

an instruction pointer queue to receive the first instruction pointers;

an instruction pointer sequencing logic/predictor component to predict a next instruction pointer for each instruction;

a micro-operation cache to store a plurality of frequently used micro-instruction operations;

a micro-operation memory to store a plurality of micro-instruction operations, said micro-operation cache to store a subset of micro-operations to be stored in said micro-operation memory; and

a trace pipe (TPIPE) to assemble micro-operations for an instruction into an instruction trace to be forwarded for execution.

38. (Previously Presented) The computer system of claim 37 wherein each of said plurality of PLAs to receive input from a build pipe that is coupled to said memory.

39. (Previously Presented) The computer system of claim 37 wherein each of said plurality of PLAs receive input from an alias logic component.

40. (Previously Presented) The computer system of claim 37 wherein said instruction pointer queue is to store said instruction pointer for said first micro-operation in each instruction.

41. (Previously Presented) The computer system of claim 37 wherein said instruction pointer sequencing logic/predictor component comprises:

a four-to-one multiplexer to receive a micro-instruction pointer from a PLA and output a micro-instruction pointer for a next micro-operation;

a micro-instruction pointer predictor to output a predicted next micro-instruction pointer to said multiplexer; and

an incrementer component to output an incremental next micro-instruction pointer to said multiplexer.

42. (Previously Presented) The computer system of claim 37 further comprising:

a patch cache to store micro-operations and to be read in parallel with said micro-operation memory.